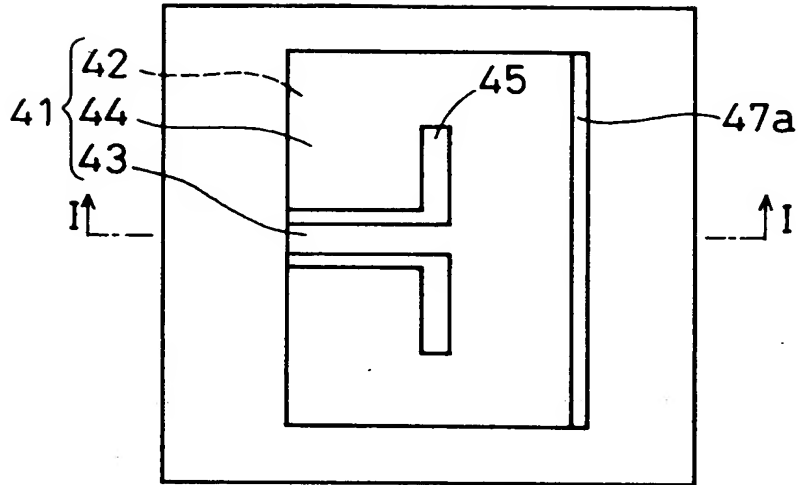
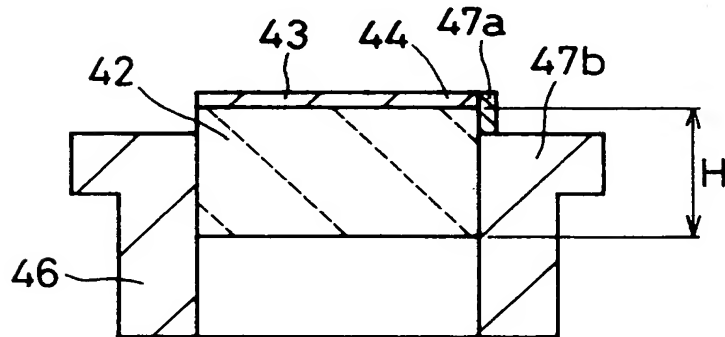


**FIG. 1A**



**FIG. 1B**



**FIG. 1C**

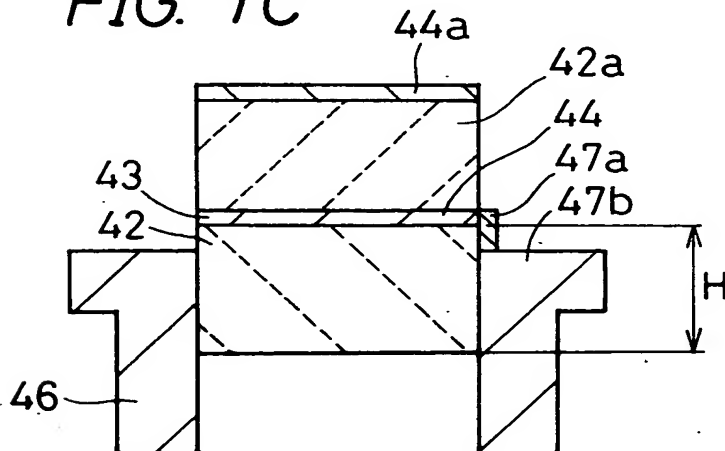


FIG. 2A

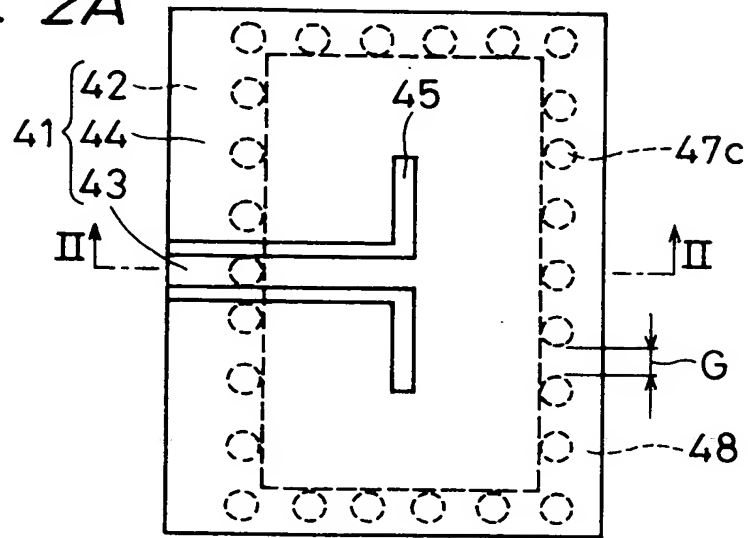


FIG. 2B

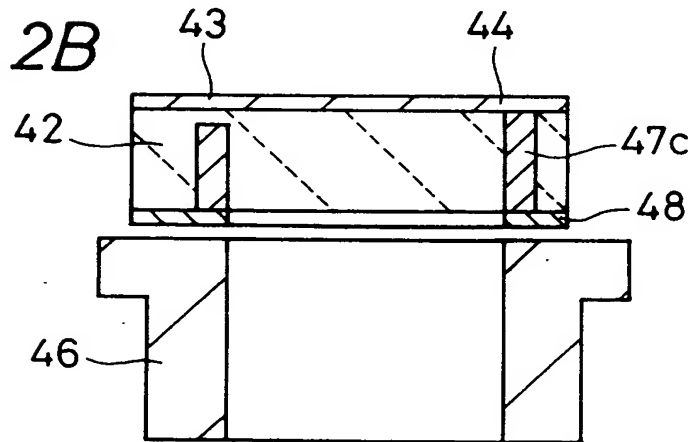


FIG. 2C

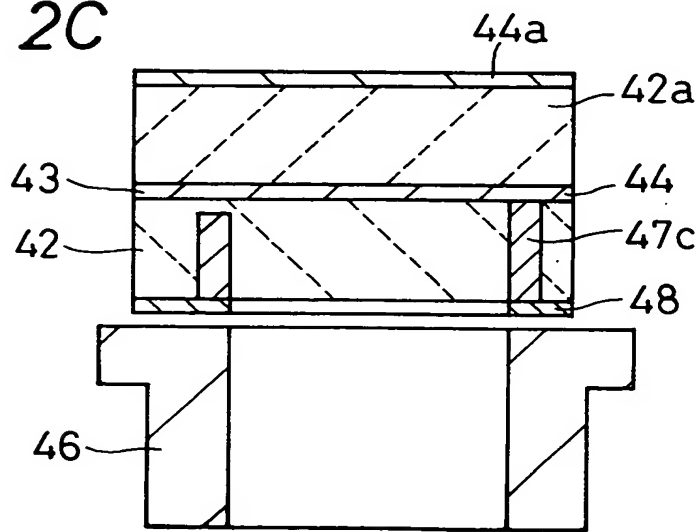


FIG. 3A

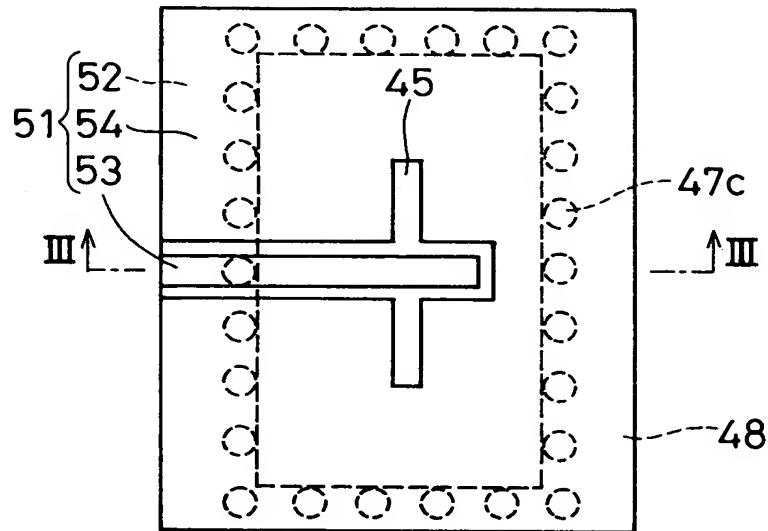


FIG. 3B

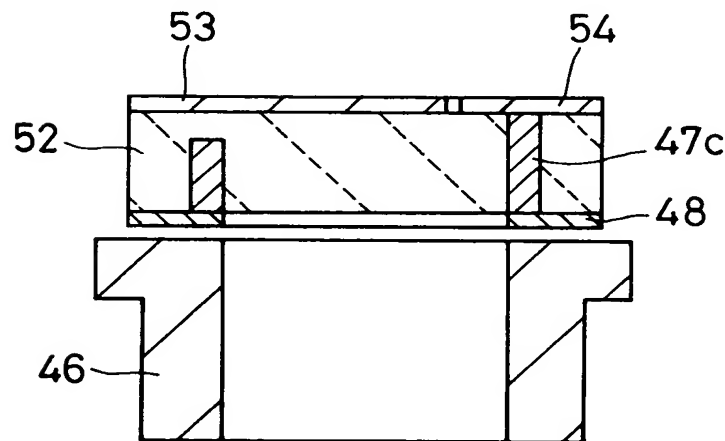


FIG. 4A

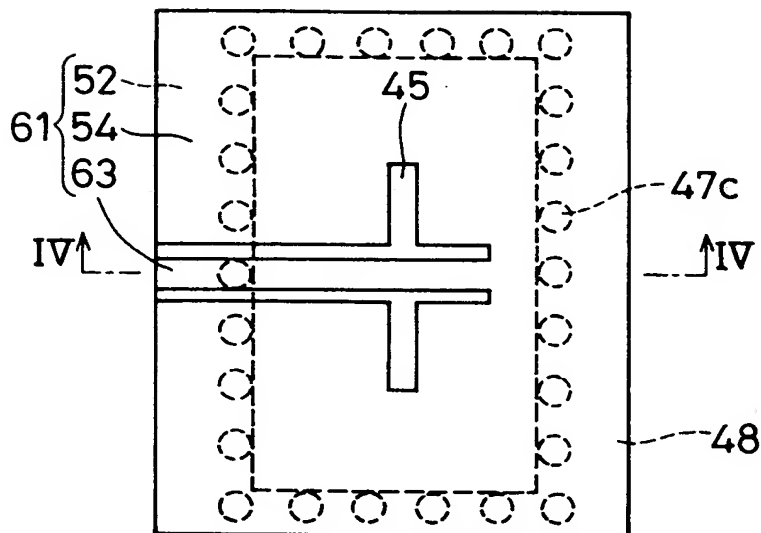
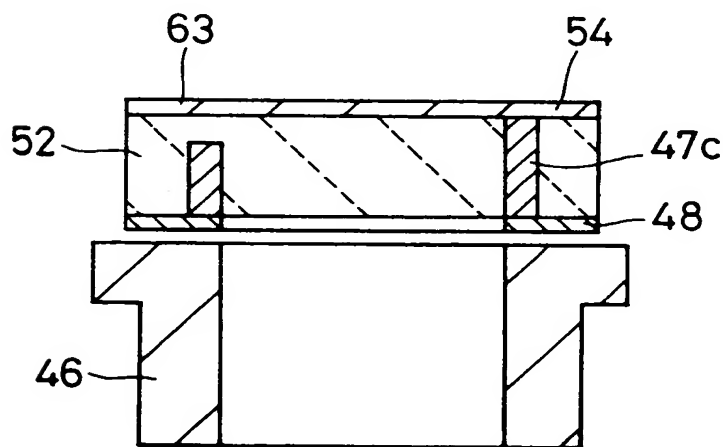
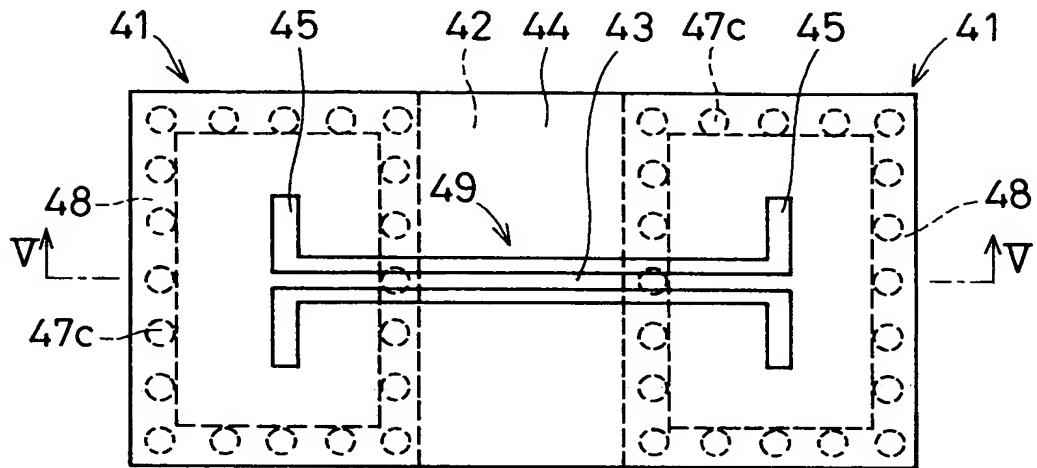


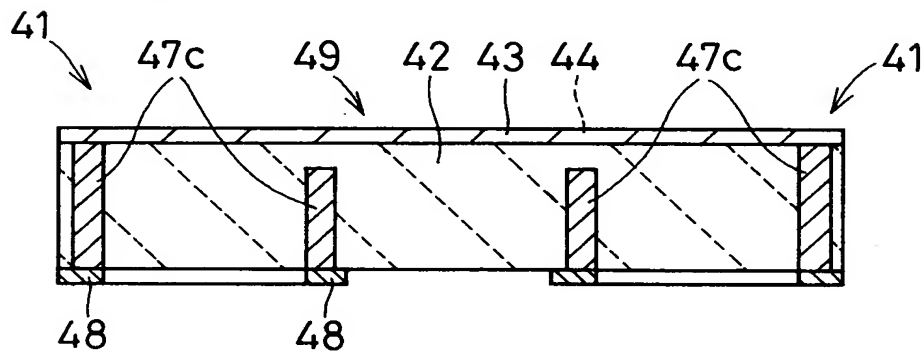
FIG. 4B



**FIG. 5A**



**FIG. 5B**



**FIG. 5C**

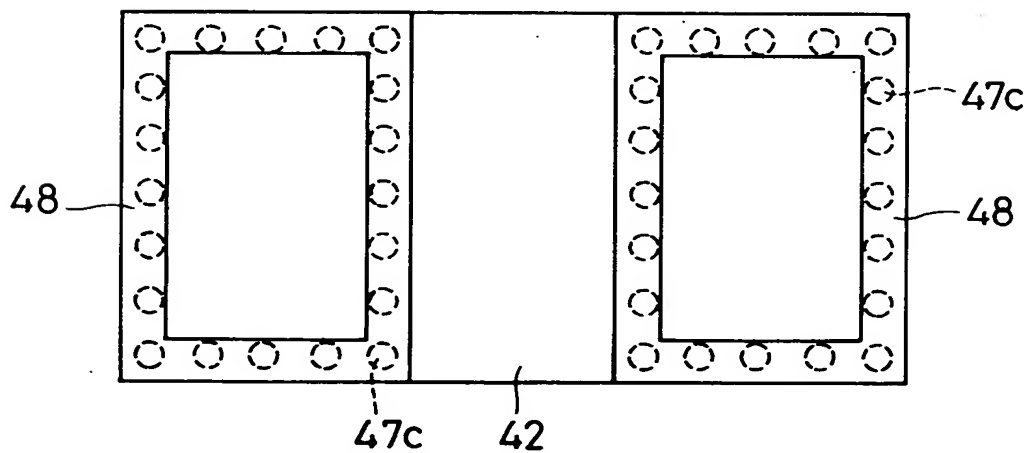
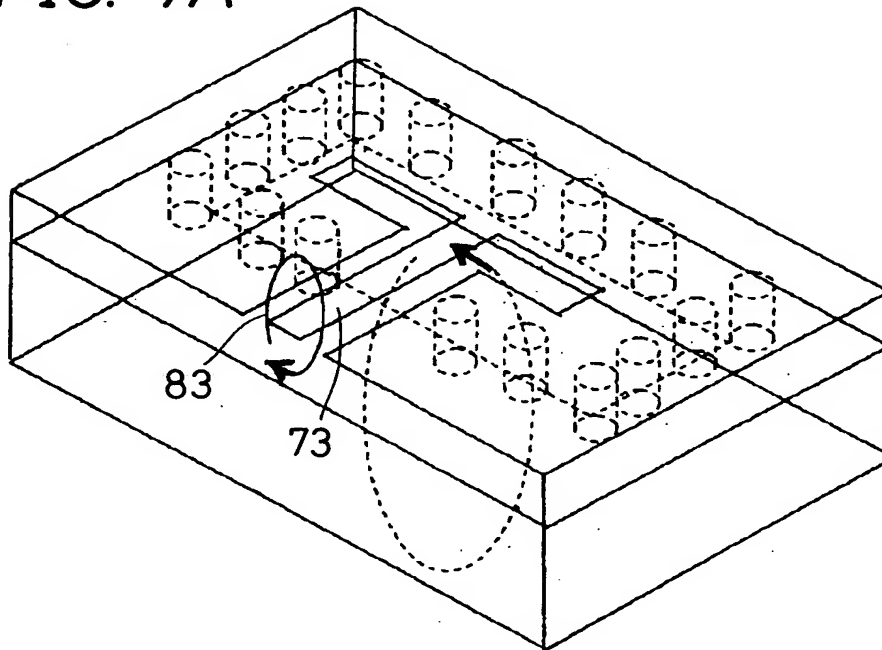


Figure 1 is a schematic diagram of a semiconductor device. It shows a central rectangular region (72) with a complex internal pattern (73, 74, 75) surrounded by a dashed rectangular boundary (76). The entire structure is enclosed within a larger rectangular frame (77). Various layers and regions are labeled with numbers 71 through 81. Arrows indicate electrical connections or signals, labeled VI and G1.

*FIG. 7A*



*FIG. 7B*

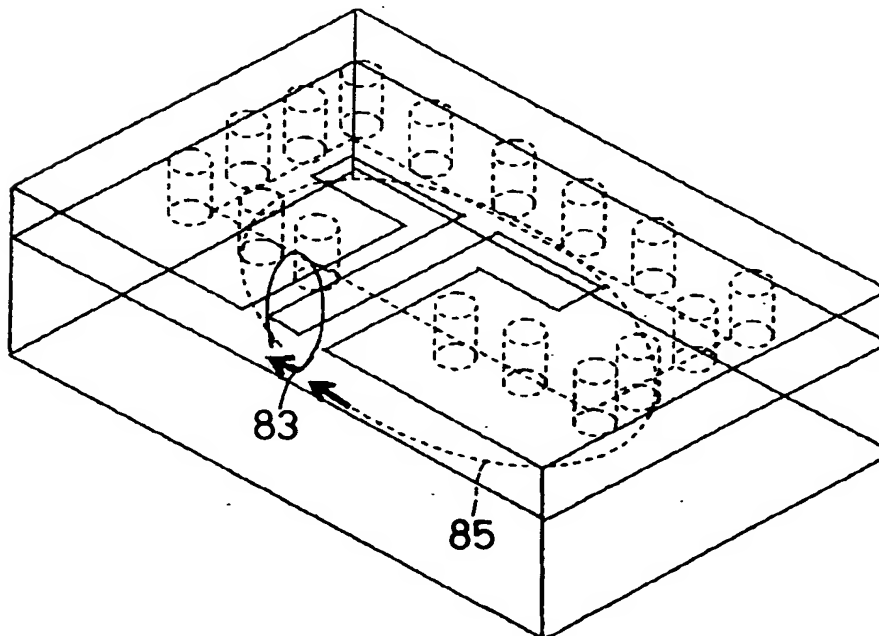
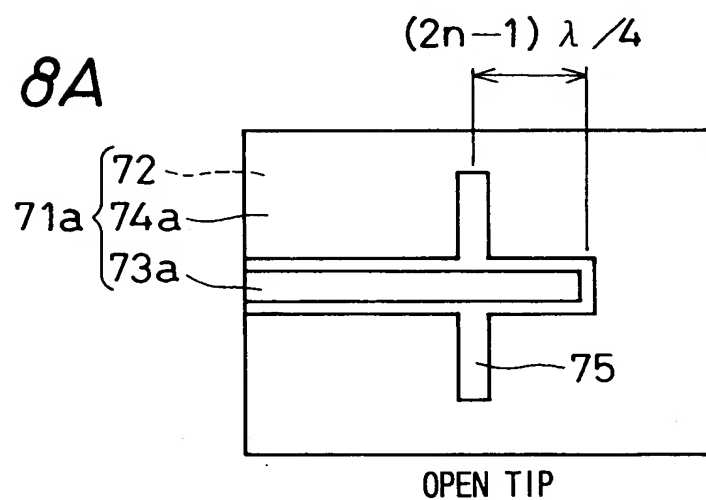
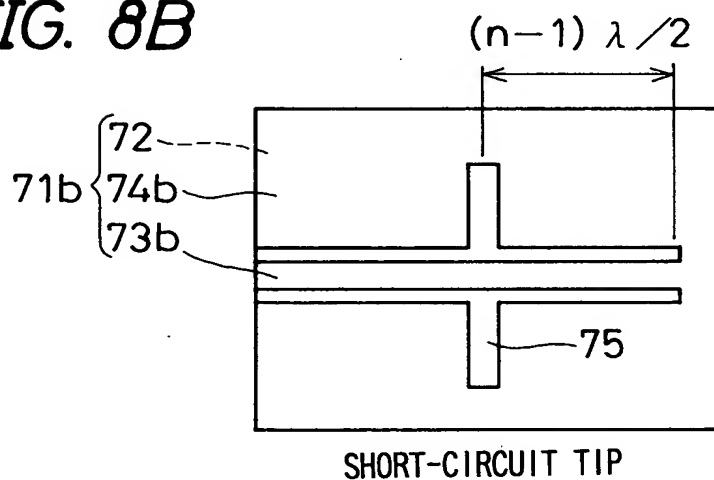


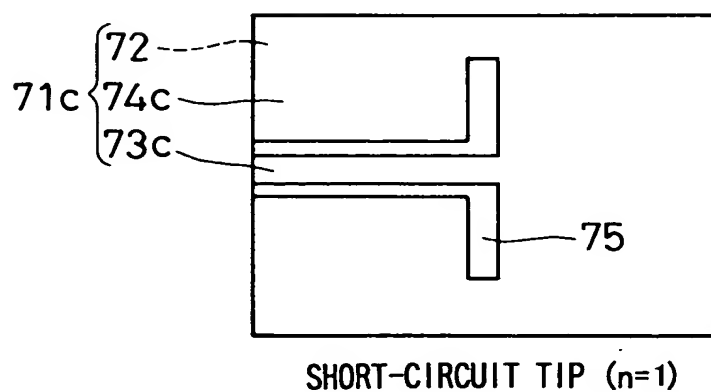
FIG. 8A



**FIG. 8B**

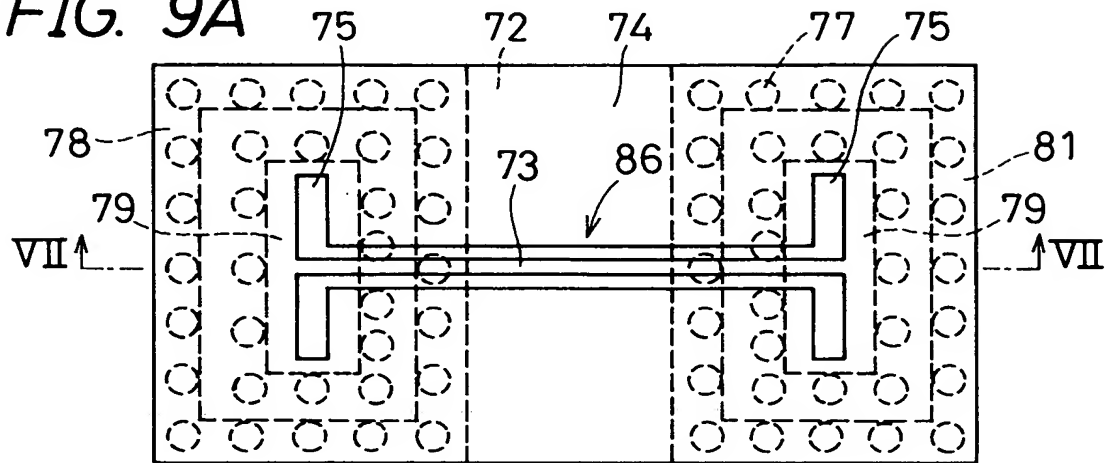


**FIG. 8C**

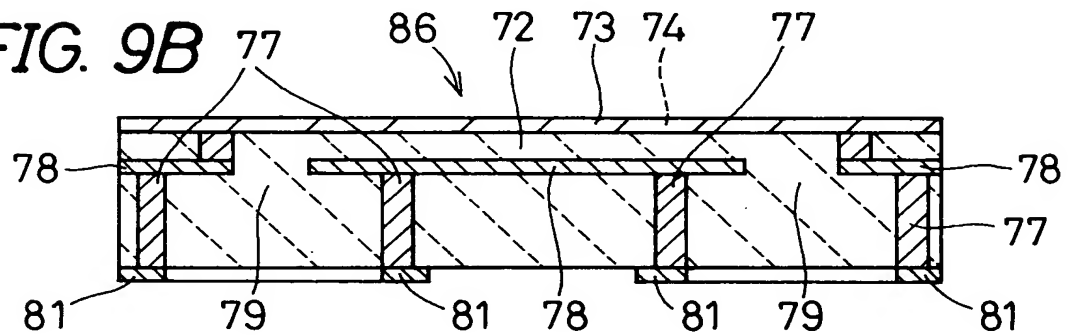




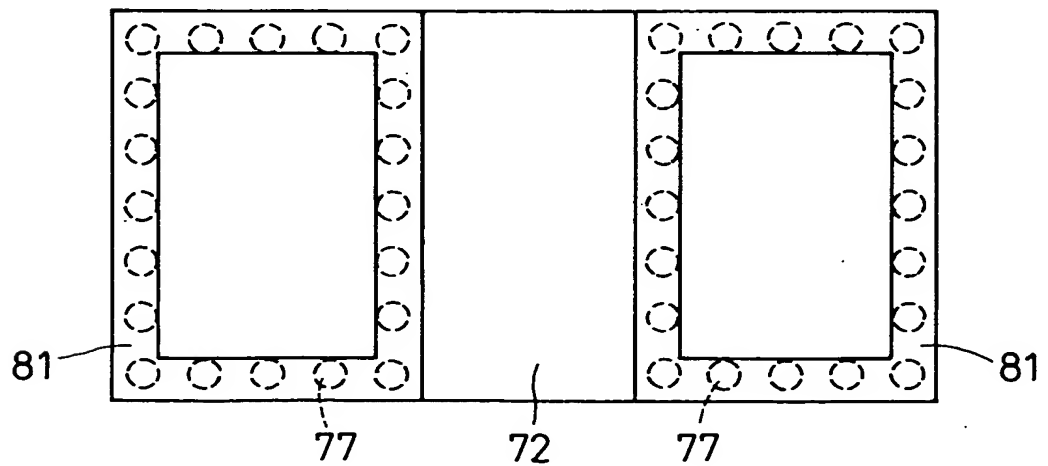
**FIG. 9A**



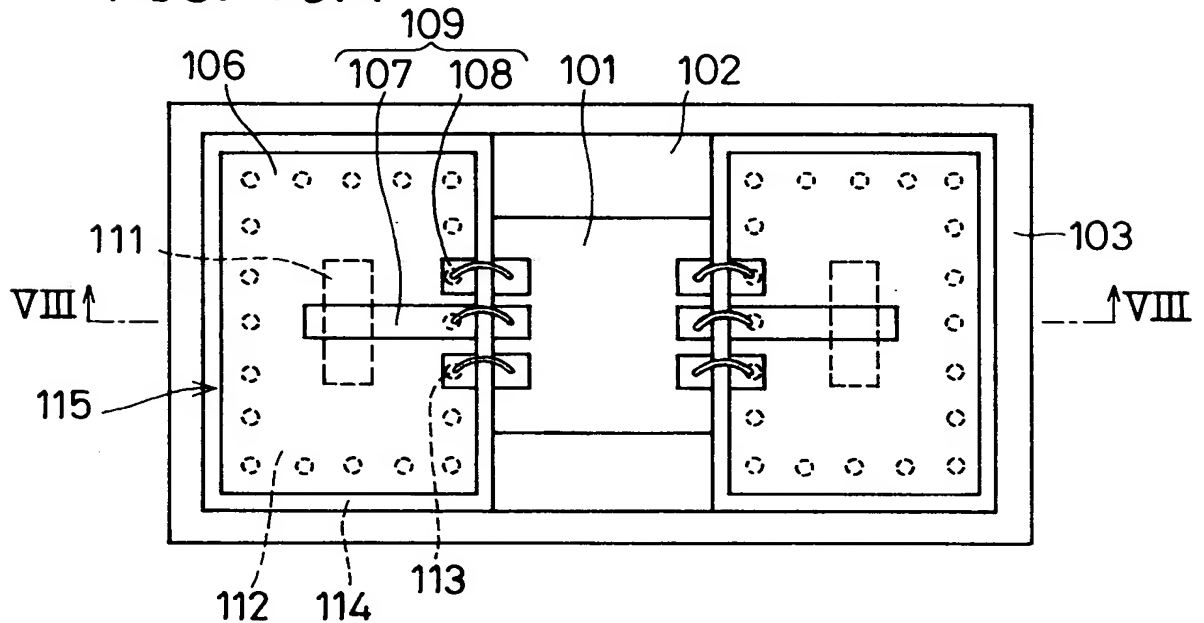
**FIG. 9B**



**FIG. 9C**



**FIG. 10A**



**FIG. 10B**

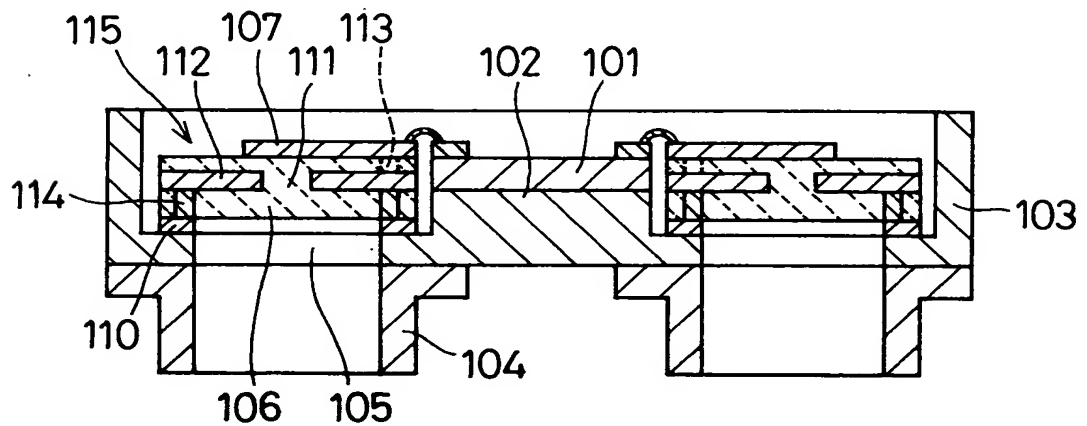
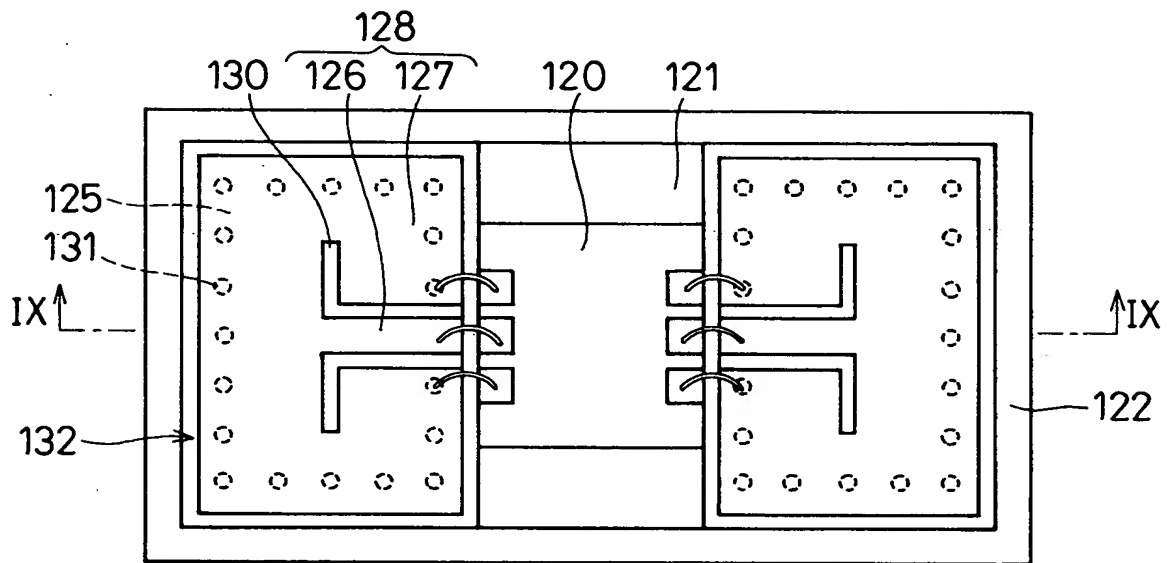
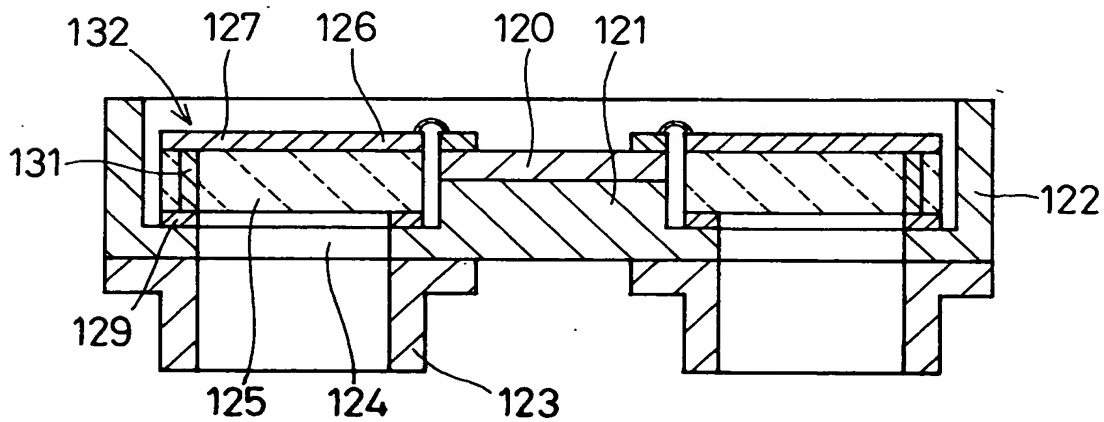


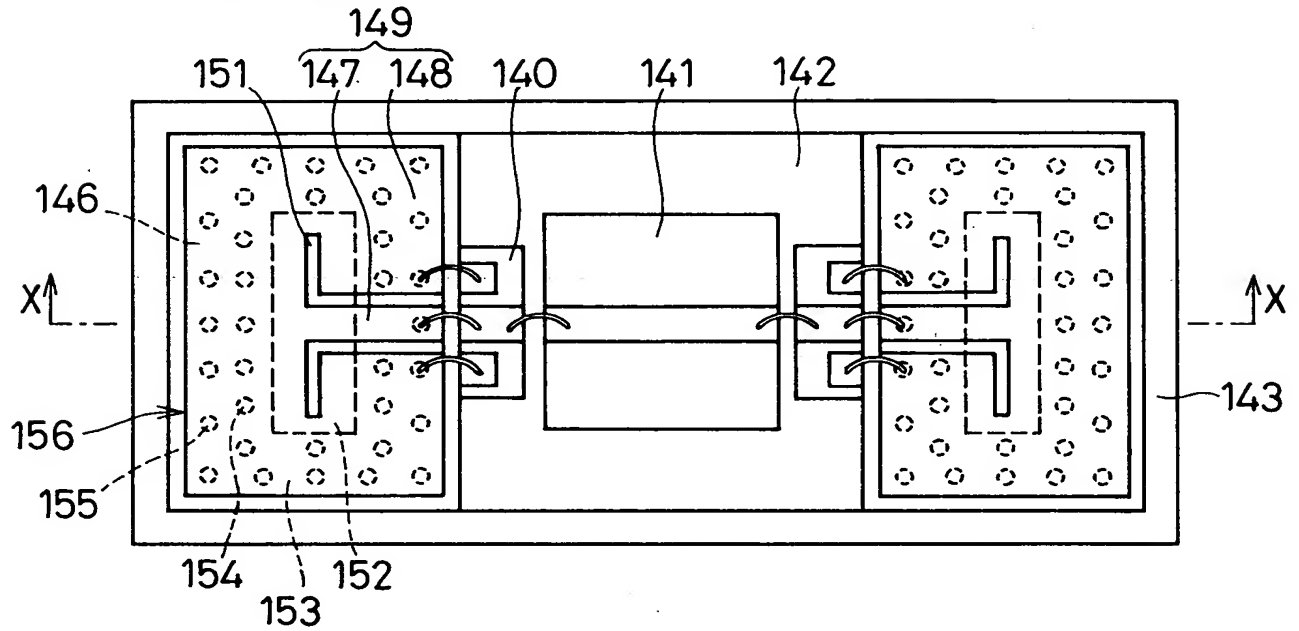
FIG. 11A



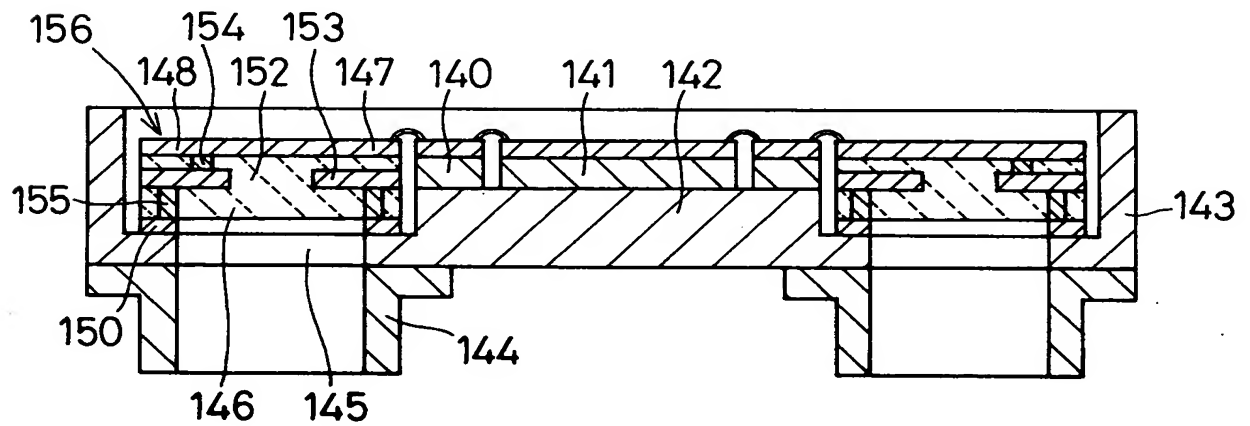
**FIG. 11B**



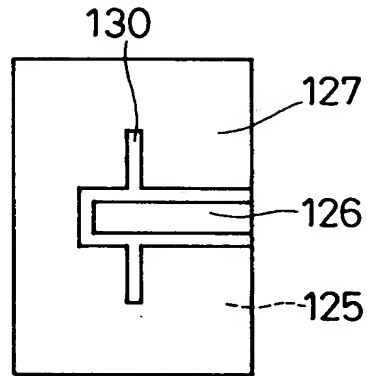
**FIG. 12A**



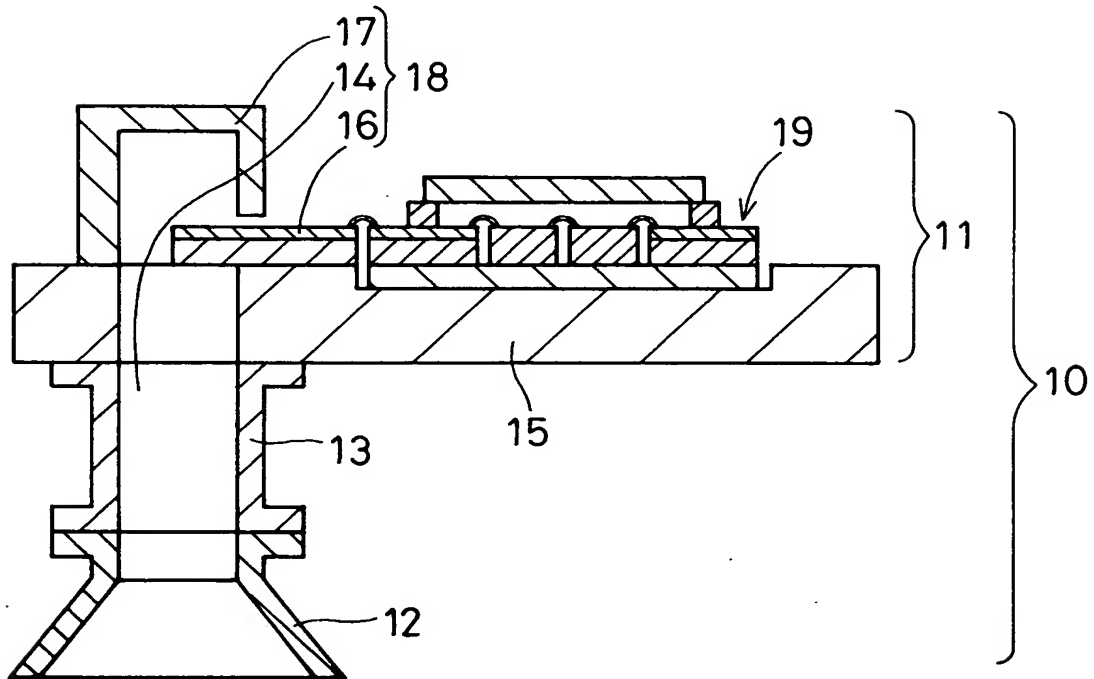
**FIG. 12B**



**FIG. 13**



**FIG. 14 PRIOR ART**



*FIG. 15 PRIOR ART*

